



NSF Future of Semiconductors Teaming Grants Webinar

Starting at 1:00 EST

Use the Q&A panel in Zoom to send questions—we'll answer some at the end

After the webinar, send questions to Fuse@nsf.gov

Live transcript is available through Zoom

Solicitation page: <https://www.nsf.gov/pubs/2022/nsf22589/nsf22589.htm>



This webinar is being recorded.

The recording, slides, and transcript will be posted on the event page within a few days.



NSF Future of Semiconductors Teaming Grant Webinar (NSF 22-589)

Thomas Kuech ENG/CMMI
Sankar Basu CISE/CCF

Solicitation page: <https://www.nsf.gov/pubs/2022/nsf22589/nsf22589.htm>

Proposals due July 18, 2022

Submit questions using
the Q&A icon in Zoom





Semiconductor Technology



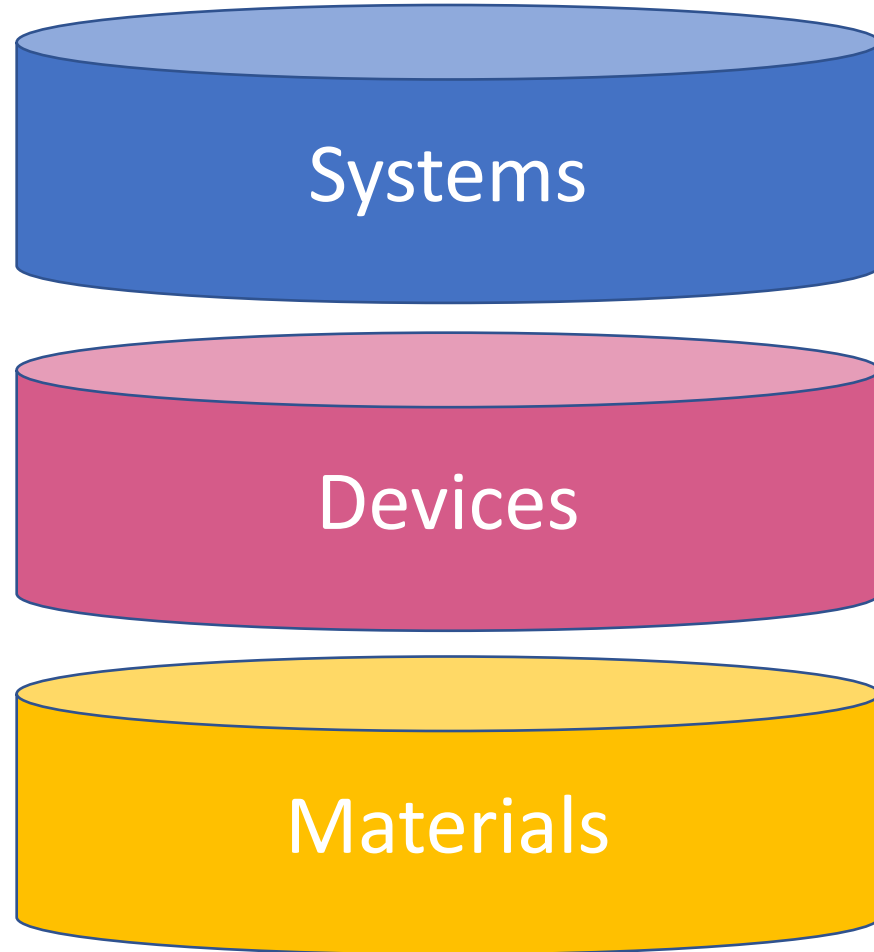
Semiconductors enable information processing that impacts all aspects of life from **computing** to **finance**, to **sustainable environment** and **healthcare**.

“It is the sense of Congress that the leadership of the United States in semiconductor technology and innovation is critical to the economic growth and national security of the United States.”

- *Senate Bill (The CHIPS Act)*



Technology Stack



Continued growth in technology requires new materials, devices and system architectures for continued growth in function and performance.

So far research in these areas occurs mostly independent of their impact and use on other aspects of the technology stack

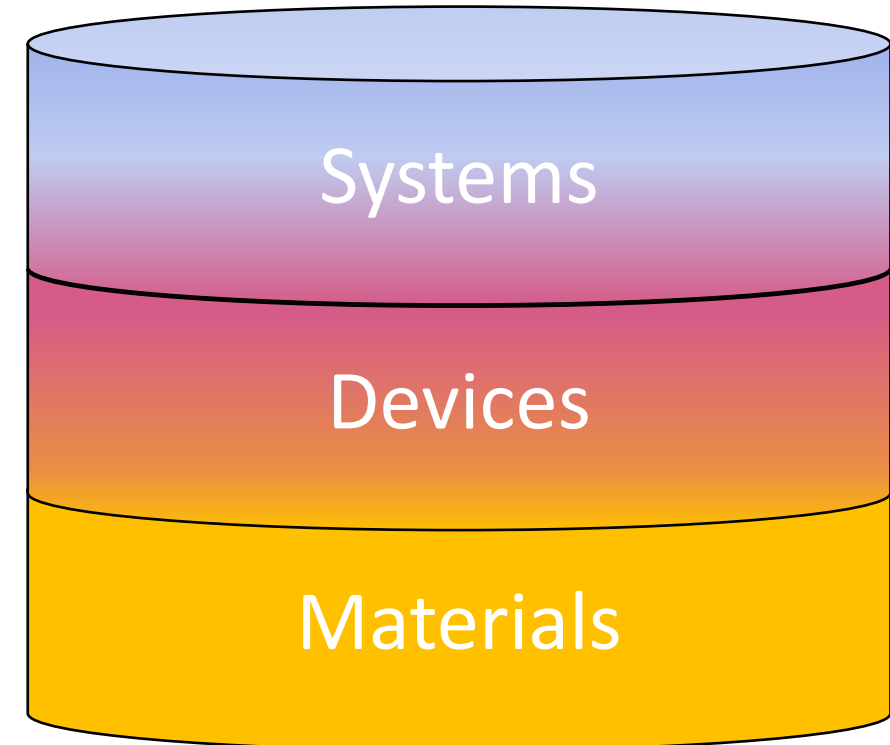
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The Future of Semiconductors

- To accelerate development of the *Next* generation of semiconductor-based technologies this independent development and uncoordinated ‘handoff’ of innovations needs to change.
- Future manufacturing will be empowered by **co-design**: materials-devices-systems where coordination and research is integrated and carried out in parallel, not in series, with a constant feedback loop between levels in the stack.



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The Future of Semiconductors

Theme

Co-Design

- Enable the breakthrough of new devices, materials, etc. that would otherwise be stranded by “chicken and egg” considerations.
- Demonstrate that the chosen co-design approach yields significant benefits.

Outcomes

- **Accelerated Innovation**
 - Improvements in Speed, Density, Security, Cost
 - Energy efficiency and Sustainability
 - Scaling: Accelerated pace of innovation over multiple generations
- **Larger and More Capable Workforce**
 - Novel educational environments that enable experiential learning of semiconductor-relevant skills
 - Diversity of learning environments (2-year and undergraduate)
 - Enhanced internship and coop program opportunities

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Teaming Solicitation

- Cultivate a broad coalition of researchers from across science and engineering communities to
 - utilize a holistic, co-design approach to fundamental research and education and training
 - to enable rapid progress in new semiconductor technologies.
- Support team-formation to articulate co-design visions for the future.
- Support capacity building across the co-design platform, which positions investigators for future competitive larger research grants and possibly future center activity.
- Expand the education and training of the next-generation workforce in the semiconductor industry

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FuSe Teaming Grants

Activities within the scope of this solicitation include but are not limited to:

- Multi-institution team formation
- Travel, student support
- Multidisciplinary workshops
- Data collection
- Preliminary experiments
- Pilot studies

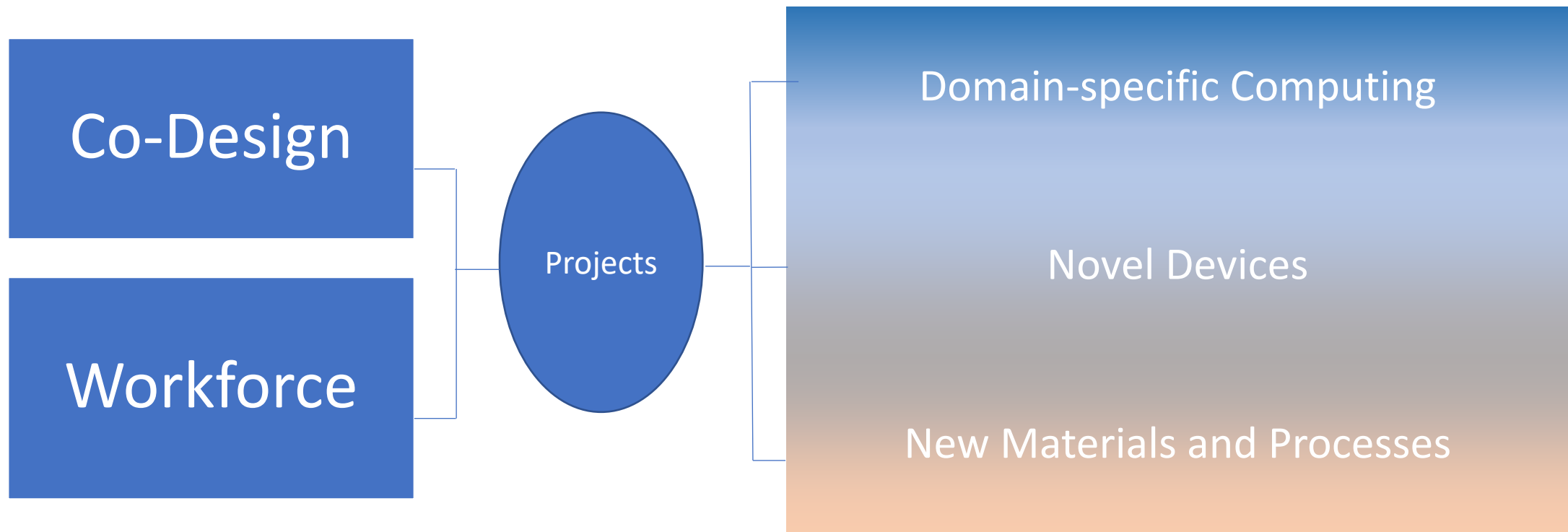
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Future of Semiconductors (FuSe) PROGRAM SOLICITATION: NSF 22-589

Future Semiconductor Leadership





FuSe Research Framework (1)

FuSe Co-design Research:

Unlock new opportunities through co-design across multiple areas of semiconductor specialization.

Examples:

- Domain-specific chip designs that leverage novel devices, materials and/or packaging
- Enabling novel devices through the use of new materials
- Chemical Processing/Manufacturing innovations that enable integration of new materials/devices

Projects must demonstrate how focused co-design across at least two areas of specialization can yield significant improvements over the anticipated baseline



FuSe Research Framework (2)

FuSe Curriculum and Workforce Development:

Inspire and expand the future semiconductor workforce through experiential learning capabilities.

- Enhance the national semiconductor workforce by broadening access to advanced capabilities.
- Tools, curriculum, online training, etc. Including access to fabrication facilities, that will facilitate the rapid diffusion of the new technologies enabled by FuSe co-design initiatives. Enable the next Mead-Conway revolution and ensure it is accessible to a wide swath of the future semiconductor workforce.

Projects must expand the potential workforce by bringing together different types of educational institutions: community colleges, minority-serving institutions, and undergraduate and graduate level college/universities.



FuSe Research Vectors (1)

Domain-Specific Computing

Increase the performances, usability, sustainability or other aspects by exploiting the characteristics of a broad domain of interest.

Example Domains:

- Applications: AI/ML; wireless next-G; sparse-data computing; AR/VR, genomic or financial computing
- Architecture: Non-von Neumann, Approximate/analog; X-inspired (X=brain, quantum, physics, bio); security and privacy-preserving
- Technology: in-memory computing; 2.5/3D; CMOS+X; probabilistic bits; Novel EDA, energy-efficient and sustainable approaches



FuSe Research Vectors (2)

Novel Devices and Hetero-integration

Accelerate adoption of robust, compact, energy-efficient and cost-effective devices. Cohesive approaches that offer ease of device implementation and ease of system integration.

- Applications: Sensing, actuation, processing, storage and communication of information
- Technology examples: Hetero-integration of electronic, photonic, RF / mixed signal, quantum, memory, energy or sensing devices (analog or digital); including integration with silicon platforms.
- Co-design considerations: Domain-specific optimization of device characteristics; Integration of new materials; Models, tools and/or manufacturing characterization that enhance predictability



FuSe Research Vectors (3)

New Semiconductor Materials and Processes

Discovery that is cognizant of the constraints under which the materials will be used with respect to: dimensions, interfaces, chemical and manufacturing processing and environmental impact.

- Applications: Scalable atomically precise material synthesis and processing for energy-efficient logic, memory, sensing and communications
- Technology examples: Materials that enable, e.g., superconductivity, spintronics, valleytronics, photonics; self-assembly processes; Atom level metrology and imaging
- Co-design considerations: Materials and manufacturing flows that enable new types of devices, including chemical processing, long-term environmental considerations



Recent Workshops

- NSF Workshop on Micro/Nano Circuits and Systems design and Design Automation: Challenges and Opportunities.
https://nsfedaworkshop.nd.edu/assets/432289/nsf20_eda_workshop_report.pdf
- Semiconductor Foundry Access by US Academic Researchers in Micro- and Nano- Circuits and Systems.
https://nsfedaworkshop.nd.edu/assets/429148/nsf20_foundry_meeting_report.pdf
- NSF Workshop on CMOS+X Technologies.
<https://e3s-center.berkeley.edu/wp-content/uploads/2022/01/CMOSX-report-Final-small.pdf>
- Future of Semiconductors Workshops: Materials and Devices/Devices and Technologies
https://nsf-fosworkshop.nd.edu/assets/455435/fos_final_report.pdf

NSF Workshop on Future of Semiconductors and Beyond: Devices & Technologies,” organized by Prof. Kang Wang (UCLA) was held February 8, 9, 17, and 18, 2021

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FuSe Award Size and Information

- Anticipated NSF-funding amount: \$10,000,000
- Award size:
 - \$100,000 per participating organization, with a minimum of at least three participating organizations per project.
- Estimated number of awards: 30
- Educational activities that focus on the skilled technical workforce and involve collaborations with two-year institutions of higher education are particularly encouraged across all Teaming Grants. The participation of minority-serving institutions in research and training is encouraged.



FuSe: Organization Eligibility/Limit

- There are no restrictions or limits on the number of proposals per organization.
- U.S. *academic institutions* which perform research and with degree-granting education programs in disciplines normally supported by NSF are eligible to be the lead organization.
- *Academic institutions* are accredited two- and four-year Institutions of Higher Education having a campus in the US, acting on behalf of their faculty.

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FuSe: PI Eligibility/Limit

- **PI Eligibility:**
Principal Investigators (PI) must be at the faculty level as determined by the submitting organization.
- Limit on Number of Proposals per PI or Co-PI: **Two** (2)
- The **first two** proposals received will be accepted and the remainder will be *returned without review*.
- Additionally, proposals submitted in response to this solicitation **may not duplicate** or be substantially similar to other proposals concurrently under consideration by **other agencies** (similar proposals will be *returned without review*).

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FuSe Review Criteria

Generic NSF review criteria will apply

- National Science Board approved Merit Review Criteria
 - **Intellectual Merit**
 - **Broader Impacts**

NSF Staff will give careful consideration to the following

- Integration of Research, Education, and Workforce development
- Integrating Diversity into NSF Programs, Projects and Activities

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Solicitation Specific Review Criteria (1)

***All FuSe* teaming grant proposals should address:**

- **Does the proposal embrace co-design linking across two or more technology areas (Materials, Devices, Systems)**
- Does the proposal present a set of activities that will prepare the team for a future proposal of appropriate scale and scope, as envisioned by the team?
- Is the proposed teaming strategy appropriate for developing a potential competitive FuSe research capacity?

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Solicitation Specific Review Criteria (2)

***FuSe* teaming proposals for center scale awards should address:**

- Does the proposed research address a complex and capacity issue for the future of semiconductors that requires co-design research at a center scale?
- Are the proposed strategies for engaging and developing the stakeholder community appropriate?
- Are minority-serving institutions, community colleges, and those organizations which contribute to research and training by focusing on the skilled technical workforce included?
- Does the proposal demonstrate a commitment to engaging underrepresented groups and diverse organization types?

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




Make the most of other institutions and activities

- Can lead or participate
 - Minority-Serving Institutions, HBCUs, HSI
 - Primarily Undergraduate Institutions
 - Community Colleges/2-yr institutions
- Partnering with:
- Industrial collaborations
- National Laboratories collaborations
- Manufacturing USA Institutes

These organizations are all qualified to participate but whether they can receive funding, see the FuSe program (NSF 22-589) solicitation and Proposal and Award Policies and Procedures Guide (PAPPG, NMSF 20-1)

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FuSe solicitation timelines

- **April 18, 2022** Program announcement
- **June 10, 2022** Information Webcast
- **July 18, 2022** Proposals Submission Deadline
- **Proposal review September 2022**
- NSF awards are expected to be made, pending availability of funds, by **December 2022**.
- A Grantee Meeting will be planned for early **2023** (applications may include travel costs in proposal budget).

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Key website Address

- Funding opportunity page with links to solicitation and announcements:
<https://www.nsf.gov/pubs/2022/nsf22589/nsf22589.htm>
- Email: FUSE@nsf.gov
- Contact program officers listed in the solicitation
- A recording and transcript of the webinar, along with the slides, will be accessible from the event page shortly after conclusion of the webinar

Q&A

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THANK YOU

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