Epitaxial Stressors on Ultrathin Silicon-On-Insulator

Eli and Peter Sutter, Colorado School of Mines, DMR-0208673

Recent trends toward replacing bulk silicon substrates in microelectronics by *thin silicon-on-insulator* (SOI) motivate our studies of the fundamental mechanical and electronic properties of this composite material.

We have discovered dramatic effects of local stress on ultrathin SOI. Placing an epitaxial Ge nanostructure as a stressor element on SOI induces a pronounced deformation of the substrate.

The induced strain in the SOI varies strongly on the nanoscale, and gives rise to large changes in its electronic structure. Our results suggest a novel route toward nanoscale band structure engineering via integration of epitaxial stressors on ultrathin SOI.

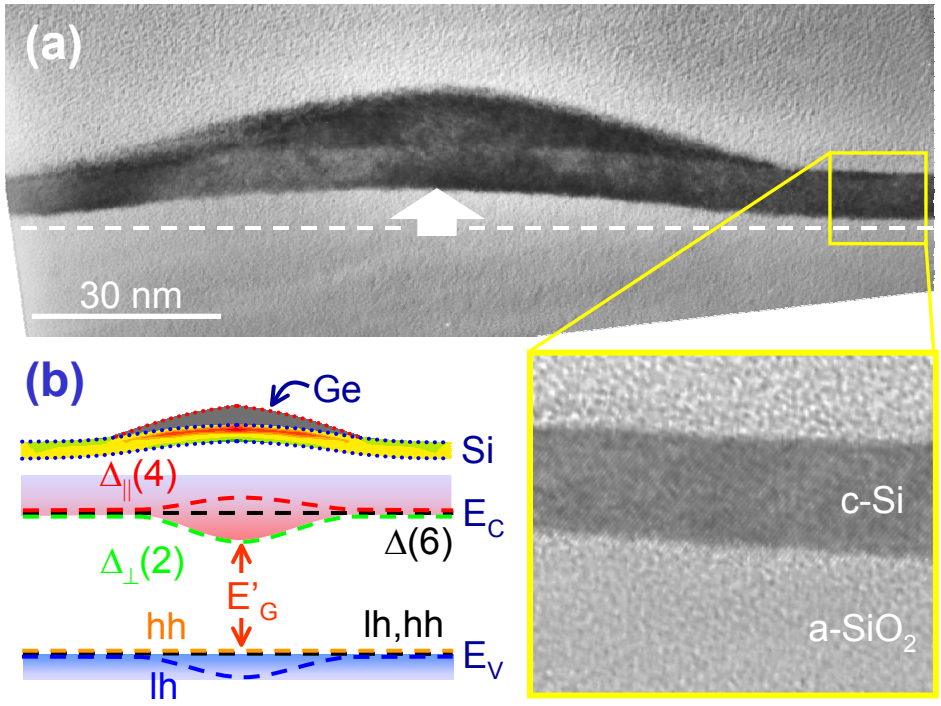

Figure 1: *(**a**) Deformation of ultrathin (7nm) SOI under lattice stress due to an epitaxial Ge stressor. **Inset:** High-resolution image of the c-Si/a-SiO_2 interface in SOI. (**b**) Nanoscale band structure engineering in locally strained SOI.*

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Education:

1 undergraduate student,1 graduate student, 1 postdoctoral researcher.

Outreach:

Developed illustrative material and hands-on activities to demonstrate research results on mechanical and electrical properties of nanostructured materials to middle school children.

Technique Development:

Developed new approaches for controlled, uniform thinning of SOI materials to below 5 nm.

Developed techniques to enable scanning tunneling microscopy on ultrathin SOI, key for studying surface processes such as etching and epitaxial growth.

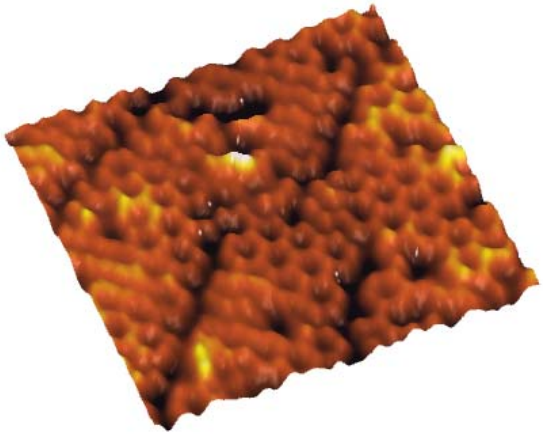

Figure 2: *Atomic resolution tunneling microscopy, 1 atomic layer of Ge on 8nm SOI.*

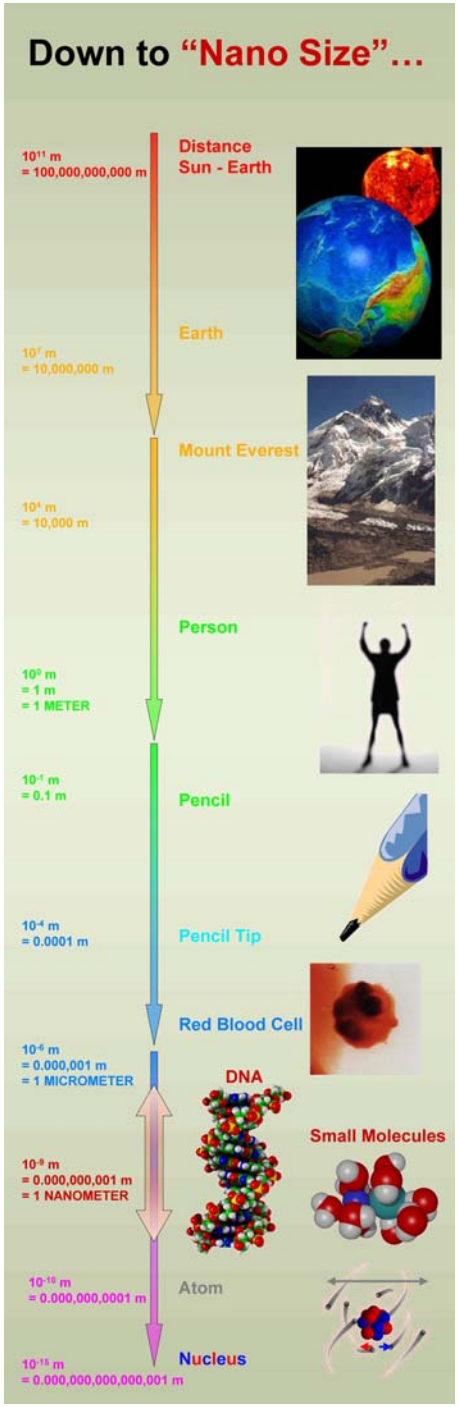

Figure 3: *Part of an illustrative poster, aiding in the demonstration of research findings under this grant to schoolchildren.*