NIRT: Semiconductor Nanowires - Building Blocks for Nanoscale Devices

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- Our work has focused on studies of intentional doping and unintentional impurities in silicon nanowires synthesized by vapor-liquid-solid (VLS) growth. The effect of dopant source reactivity on the structure of the nanowires was investigated. The use of diborane for p-type doping, which reacts readily with silane, leads to highly defective wires with a thick amorphous Si shell (Fig. 1a) while single crystal wires (Fig. 1b) were obtained using trimethylboron (TMB), a less reactive source.
- A four-point electrical test structure (Fig. 2) was developed and used to measure nanowire resistivity and determine carrier type via gated I-V measurements. Nanowire resistivity decreased with the addition of intentional dopants (Fig. 3). Undoped nanowires were found to be p-type and the unintentional acceptors fully compensated donors at low n-type doping levels. The background p-type conductivity is characteristic of silicon nanowires grown by VLS using gold as the catalyst.

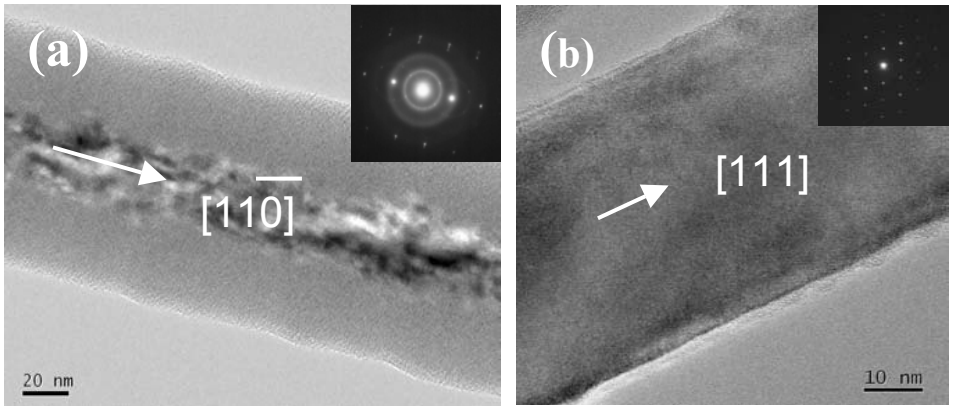

Figure 1. TEM images of silicon nanowires doped using (a) diborane and (b) trimethylboron.

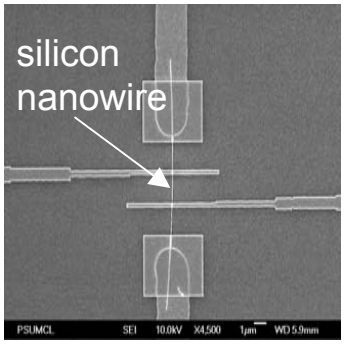

Figure 2. Four point electrical test bed.

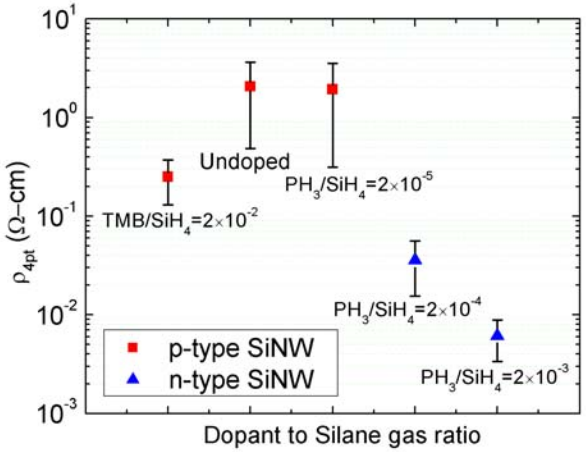

Figure 3. Nanowire resistivity versus doping level.

Aims of the project:

Silicon nanowires, synthesized by vapor-liquid-solid (VLS) growth, are of interest for nanoscale devices including gate-all-around transistors and chemical and biological sensors fabricated using a bottom-up assembly approach. Our research is focused on understanding the effect of wire diameter, intentional doping and surface passivation on carrier transport in nanowires. This work involves the development of new processing technology to synthesize, contact and electrically characterize nanowire structures.

Research results:

Our recent work has focused on studies of intentional doping and unintentional impurities in silicon nanowires. Our studies have illustrated the importance of understanding the effect of dopant source chemistry and dopant incorporation on nanowire structure. The use of diborane, a common source for p-type doping of silicon thin films, produces highly defective nanowires with a thick amorphous silicon shell (Fig. 1a). The use of trimethylboron eliminates this problem and enables the growth of single crystal nanowires (Fig. 1b) even at high boron concentrations ([B]~$1x10^{19}$ cm^{-3}). The different nanowire structures can be explained by comparing the thermal stability and reactivity of the two dopant sources. Diborane (B_2H_6) decomposes at lower temperatures than trimethylboron forming monoborane (BH_3) which reacts with silane (SiH_4) leading to an enhancement in the silicon thin film deposition rate. The increased silicon thin film deposition rate results in the formation of an amorphous silicon layer on the outer surface of the nanowire as it grows in length. Controlled n-type doping was also demonstrated using phosphine as the dopant source.

A four-point electrical test structure (Fig. 2) was developed and used to measure nanowire resistivity and determine carrier type via gated I-V measurements. The test structure was fabricated by integrating the nanowires via electrofluidic alignment onto thermally oxidized Si substrates with lithographically defined electrodes. Topside source and drain contacts and two additional voltage probes were patterned in double layer PMMA/polymer resist using electron-beam lithography followed by liftoff of Ti(80 nm)/Au(200 nm) deposited by thermal evaporation. Four-point resistivity measurements were carried out by applying a current between the two large area source and drain contacts and measuring the differential voltage that developed across two internal voltage probes to obtain resistance. The nanowire resistivity was then determined from the measured resistance using values for nanowire diameter and length obtained from field-emission scanning electron microscopy. Nanowire resistivity decreased, in general, with the addition of both p-type and n-type dopants (Fig. 3). Carrier type (n or p) was determined from the change in drain to source current (I_{DS}) as the gate voltage (V_{GS}) applied to the backside of the silicon substrate was varied from zero to positive (p) or negative (n) values. The undoped, boron doped and lowest phosphorus-doped nanowires showed a decrease in I_{DS} as V_{GS} was increased from 0 to +5V, which is consistent with depletion

low n-type doping levels and increased phosphorus levels were required to obtain n-type conductivity. Our results demonstrate that background p-type conductivity is characteristic of silicon nanowires grown by VLS using gold as the catalyst.

Significance of this work:

Despite the growing interest in silicon nanowires for applications in nanoelectronics and sensing, little is known about their basic electrical properties. Our work has identified processing conditions and suitable dopant sources for controlled p-type and n-type doping of VLS-grown silicon nanowires. We have demonstrated that unintentional acceptors are present in nominally undoped silicon nanowires grown by VLS using gold as the catalyst giving rise to background p-type conductivity. These acceptors fully compensate donors at low n-type doping levels and increased levels of phosphorus are necessary to achieve n-type conductivity. These results were used to demonstrate complementary p- and n-channel depletion mode silicon nanowire field-effect transistors.

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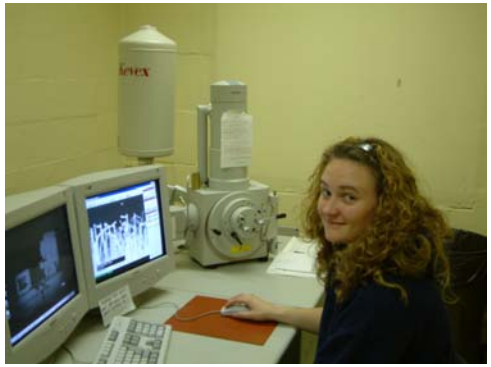
Education:

Eight graduate students, one post-doctoral scholar and eight undergraduate students participated in the project during the past year. The graduate students are pursuing advanced degrees in materials science and engineering, electrical engineering and physics. During the past two summers, six undergraduate REU students worked in our labs and two students carried out related projects during the year for their senior thesis.



REU student Sarah Dilts uses a scanning electron microscope to characterize nanowire samples.

Outreach:

A workshop on light emitting diodes was offered to 20 high school students participating in GUTS (Girls Utilizing Science and Technology) camp at Penn State. Selected workshop activities were incorporated into a lesson plan for 7th graders at St. John's School in Bellefonte, PA. Additional activities included demonstrations of low temperature physics and electronic and photonic materials to students attending science and career fairs at Penn State.

The PI discusses materials used in light emitting diodes with students and parents attending EMEX 2004 at Penn State.