NATIONAL SCIENCE FOUNDATION
2415 EISENHOWER AVENUE
ALEXANDRIA, VIRGINIA 22314

NSF 22-076

Dear Colleague Letter: Partnership for Prototyping of CMOS+X Systems

April 22, 2022

Dear Colleague:

The National Science Foundation recognizes the opportunity to drive system-level performance improvements in computing and communications by integrating CMOS semiconductor chips with emerging technologies. Examples of promising emerging technologies include, but are not limited to, resistive and nanomagnetic memories and novel transistors based on ferroelectric or 2D materials. The promise of these emerging technologies has not been fully realized, in part because of barriers to collaboration between materials scientists who investigate novel materials and heterostructures, device researchers who model device characteristics, and computer system designers who create new circuits and architectures through simulation. Additionally, lack of access to fabrication facilities also poses a problem of co-integration of CMOS with emerging (X) technologies. Such barriers have been brought into focus by recent workshops exploring "CMOS+X" approaches funded by the National Science Foundation. See, for example, https://nsfedaworkshop.nd.edu/foundry-meeting/ and https://e3s-center.berkeley.edu/nsf-workshop-cmosx/cmos-x-report/.

As a step towards overcoming these barriers, this Dear Colleague Letter (DCL) invites proposals for CMOS+X technology demonstrations from teams bringing together device researchers and computer system designers. For example, a team might bring together one group (e.g., material scientists and device researchers) with infrastructure or access to fabricate an emerging technology (X) that can be co-integrated with CMOS at a low granularity level on the one hand — with another group (system designers) with expertise in designing fabless CMOS+X systems and demonstrating advantages of emerging technologies using device modeling and circuit simulation on the other. Collaborations between two or more organizations are strongly encouraged to prototype, test, and evaluate CMOS+X integrated circuits, and thereby to broaden the set of researchers engaged in these efforts. Cointegration of larger functional blocks may also be attempted depending on

available facilities. This pilot effort is to plan for the integration of emerging technologies on CMOS substrates to push the frontier of semiconductor technology and chip fabrication. Therefore, the proposals should aspire for outputs including fabricated CMOS+X chips and well-characterized systems, as well as related toolchain and workflow results.

PROPOSAL PREPARATION AND SUBMISSION

Proposals in response to this DCL may be submitted to several programs:

- In the Directorate for Computer and Information Science and Engineering (CISE), proposals may be submitted to the the existing NSF/CISE core program solicitation (NSF 21-616) in the Small project category. Proposals may be submitted to the Foundations of Emerging Technologies cluster or the Software and Hardware Foundations cluster of the Division of Computing and Communication Foundations (CCF).
- In the Directorate for Mathematical and Physical Sciences, proposals may be submitted to the Electronic and Photonics Materials (PM) Program (NSF 21-600) of the Division of Materials Research (DMR).
- In the Directorate for Engineering, proposals may be submitted to the Electronics, Photonics and Magnetic Devices (EPMD) Program (PD 18-1517) or the Communications, Circuits, and Sensing Systems (CCSS) Program (PD 18-7564) of the Division of Electrical, Communications, and Cyber Systems (ECCS); or to the Advanced Manufacturing (AM) Program (PD 19-088Y) of the Division of Civil, Mechanical, and Manufacturing Innovation (CMMI).

Proposals must follow the general guidelines of the targeted program as described in their respective funding opportunities, or their future revisions as appropriate. Specifically, a proposal must meet the deadlines, budgetary requirements, and review criteria of the respective programs, and must include the prefix "CMOS+X:" in the proposal title after any program-specific title requirements.

PI teams must consist of more than one investigator with appropriately complementary expertise. Collaborative projects from more than one organization are strongly encouraged. Each project must clearly demonstrate substantial collaborative contributions of interest to the respective communities.

Types of allowed costs may include but are not limited to: (a) cost of fabrication of CMOS wafers, including the cost of Multi Project Wafer (MPW) service providers, cost of design tools, cost of testing, etc.; (b) cost of integration of X devices on CMOS wafers at the fabrication facility, and cost of testing; and (c) student support for training at the fabrication facility, etc. Proposals must provide a detailed breakdown of these and other such expenses related to the project. The choice of fabs/facilities for wafer and integration is left to the

proposing teams, but successful proposals are expected to provide the plan in as much detail as possible.

Extensive support for preliminary design is not anticipated to be within the purview of this DCL. Principal investigators are encouraged to leverage prior work, or support from other sources including other NSF grants, on design efforts. Inclusion of voluntary committed cost sharing is prohibited.

Questions concerning this Dear Colleague Letter should be directed to program directors Sankar Basu or Pinaki Mazumder of CCF; Paul Lane of DMR; Rosa Lukaszew or Premjeet Chahal of ECCS; or Thomas Kuech of CMMI at: CMOSPlusX@nsf.gov.

Sincerely,

Margaret Martonosi, Assistant Director
Directorate for Computer and Information Science and Engineering (CISE)

Sean L. Jones, Assistant Director
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